CLAIMS

What is claimed is:

1. A DMOS transistor source structure, comprising:
   a source diffusion;
   a gate which is capacitively coupled to control majority carrier flow from said source diffusion through a body diffusion into a semiconductor drift region; and
   an ohmic connection structure which is
      at least partly self-aligned to said body diffusion,
      positioned to collect minority carrier flow from said drift region,
      and connected to divert said minority carrier flow to bypass any junction between said source and body diffusions.

2. The structure of Claim 1, further comprising a drain region which is laterally separated from said body diffusion by said drift region.

3. An n-channel DMOS transistor source structure, comprising:
   an n-type source diffusion;
   means for controlling electron flow from said source diffusion into a semiconductor drift region; and
   means for collecting hole flow from said drift region, and for diverting said hole flow to bypass said source diffusion and thereby avoid secondary electron current.

4. The structure of Claim 3, further comprising a drain region which is laterally separated from said means for controlling electron flow by said drift region.

5. The structure of Claim 3, wherein said means for controlling electron flow comprises a p-type channel region which is capacitively coupled to a conductive gate structure.

6. An n-channel DMOS transistor source structure, comprising:

an n-type source diffusion;

a p-type surface body diffusion which laterally surrounds at least part of said source diffusion;

a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein; and

a p-type buried body diffusion which diverts at least some hole current to at least partially bypass said surface body diffusion.

7. The structure of Claim 6, further comprising a drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

8. The structure of Claim 6, wherein said buried body diffusion is self-aligned to at least part of said source diffusion.

9. The structure of Claim 6, further comprising a drain structure which includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion, and which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

10. An n-channel DMOS transistor source structure, comprising:

an n-type source diffusion, ohmically connected to a source metallization;

a p-type surface body diffusion which laterally surrounds at least part of said source diffusion;

a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein;

a p-type buried body diffusion which underlies said channel and at least part of said surface body diffusion; and

at least one additional p-type diffusion component which reduces the resistance between said buried body diffusion and said source metallization;

whereby said buried body diffusion diverts hole current to avoid parasitic bipolar turn-on and thereby increase the safe operating area of the device.

11. The structure of Claim 10, further comprising a drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

12. The structure of Claim 10, wherein said buried body diffusion is self-aligned to at least part of said source diffusion.

13. The structure of Claim 10, further comprising a drain structure which includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion, and which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

14. An n-channel DMOS transistor source structure, comprising:

an n-type source diffusion, ohmically connected to a source metallization;

a p-type surface body diffusion which laterally surrounds at least part of said source diffusion;

a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein;

a p-type buried body diffusion which underlies said channel and at least part of said surface body diffusion; and

an ohmic connection between said buried body diffusion and said source metallization;

whereby said buried body diffusion diverts hole current to bypass said source diffusion, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the device.

15. The structure of Claim 14, wherein said ohmic connection comprises a further p+ diffusion which is self-aligned to said source metallization within an aperture in said gate structure.

16. The structure of Claim 14, further comprising a drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

17. The structure of Claim 14, wherein said buried body diffusion is self-aligned to at least part of said source diffusion.

18. The structure of Claim 14, further comprising a drain structure which includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion, and which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

19. A lateral DMOS transistor, comprising:

a first-conductivity-type source region;

a second-conductivity-type surface body region, underlying and laterally surrounding said source region;

a gate electrode extending over at least a portion of said body region to define a channel region therein; and

a drain region which is part of a continuous semiconductor body with said source region, and which is separated from said source region by at least said channel region; and

a second-conductivity-type deep body region underlying said source and surface body regions;

wherein the body region provides a low impedance path for holes emitted at or near said drain region.

20. The transistor of Claim 19, wherein said conductive body region is the first conductivity type.

21. The transistor of Claim 19, wherein said conductive body region is formed by a high-energy implant into said first region.

22. The transistor of Claim 19, wherein said conductive body region is a buried layer.

23. A lateral DMOS transistor, comprising:

a semiconductor layer;

a first region of a first conductivity type formed in the semiconductor layer;

a source region of a second conductivity type opposite the first region;

a channel region defined between an edge of the source region and an edge of the first region;

a drain region of the second conductivity type formed in the semiconductor layer, the drain region adjacent the channel region;

a field oxide region formed on the first region between the source region and the channel region;

at least one gate extending over at least a portion of the channel region, the gate formed upon a gate oxide layer; and

a conductive body region in the first region and underneath the source region, wherein the body region provides a low impedance path for holes emitted at the drain region.

24. The transistor of Claim 23, wherein said conductive body region is the first conductivity type.

25. The transistor of Claim 23, wherein said conductive body region is formed by a high-energy implant into said first region.

26. The transistor of Claim 23, wherein said conductive body region is a buried layer.

27. A method for fabricating a lateral DMOS transistor, comprising:

forming a first region of a first conductivity type on a semiconductor layer;

forming a buried body region in the first region;

forming a source region of a second conductivity type opposite the first region, the source region formed such that the body is proximate the source region, and wherein a channel region is formed between an edge of the source region and an edge of the first region;

forming a drain region of a second conductivity type in the semiconductor layer, the drain region adjacent the channel region; and

forming at least one gate extending over at least a portion of the channel region.

28. The method of Claim 27, wherein said action of forming a conductive body region in the first region is forming a conductive body region of the first conductivity type in the first region.

29. The method of Claim 27, wherein said action of forming a conductive body region in the first region is implanting a conductive body region into the first region with a high energy implanter.

30. The method of Claim 27, wherein said action of forming a conductive body region in the first region is forming a conductive body region between epitaxial layer growth steps.

31. The method of Claim 27, further including the steps of:

forming one or more field oxide regions on the semiconductor layer; and

forming a gate oxide region on the first region, the channel region, and the source region,

wherein the step of forming at least one gate extending over at least a portion of the channel region is forming at least one gate upon the gate oxide region and a field oxide region.

32. A product produced by the method of Claim 27.